AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 – 5 (cancelled).

Claim 6 (presently amended). A multi-chip module comprising:

a multilayer thin-film polymeric interconnect structure formed on a semiconductor layer, said interconnect structure having a first side and a second side, said second side being adjacent to said semiconductor layer;

a chip disposed on the first side;

wherein said ~~a~~ semiconductor layer comprises ~~disposed directly on the second side and including~~ active or passive devices.

Claim 7 (original). The multi-chip module of Claim 6 wherein the active devices comprise SRAMs and wherein the passive devices comprise chip capacitors.

Claim 8 (original). The multi-chip module of Claim 6 wherein the semiconductor layer further comprises an aperture extending through the layer.

Claim 9 (original). The multi-chip module of Claim 8 wherein the aperture is filled with solder.

Claim 10 (currently amended). A multichip module substrate capacitor structure comprising:

a semiconductor substrate having a top surface and a bottom surface;

a doped region of the substrate located at the substrate's top surface;

an ohmic contact located on the top surface of the substrate, and a first dielectric layer disposed over the doped region;

a first conductive layer having a top surface and a bottom surface, and being disposed over the first dielectric layer with its bottom surface adjacent to the first dielectric layer, said first

conductive layer having at least a sub-layer of a first conductive material disposed at its top surface;

a second dielectric layer disposed over the first conductive layer;

an aperture formed in the second dielectric layer and disposed over the first conductive layer to expose a portion thereof;

a conductive via formed through the aperture and disposed against a portion of the first conductive layer and comprising a second conductive material disposed adjacent to the sub-layer of first conductive material of said first conductive layer, the portion of said second conductive material adjacent said first conductive material being different from said sub-layer of said first conductive material; and

a second conductive layer having a top surface and a bottom surface, and being disposed over the second dielectric layer with its bottom surface adjacent to second dielectric layer, said second conductive layer having a portion therefor disposed over the conductive via.

Claim 11 (original). The module of Claim 10 wherein said first conductive layer comprises polysilicon and a top layer of aluminum.

Claim 12 (currently amended). The module of Claim 10 wherein the doped region ~~comprises a top dope layer formed~~ extends over substantially the entire top surface of the substrate.

Claim 13 (original). The module of Claim 10 wherein said substrate comprises a doping level of more than 1×10^{-18} cm^{-3} and wherein the doped region is provided by the entire substrate.

Claim 14 (original). The module of Claim 10 wherein said first dielectric layer comprises silicon oxide.